6. (Amended) The system of claim 5 wherein the signal conditioning stage comprises a switched capacitor filter stage.

A5 Cont'd

7. (Amended) The system of claim 5 wherein the DAC comprises a switched capacitor DAC.

8. (Amended) The system of claim 5 wherein the magnitude of the output data rate of the DAC is at least twice the magnitude of the input data rate of the DAC.

9. (Amended) The system of claim 5 wherein the magnitude of the output data rate of the DAC is two times the magnitude of the input data rate of the DAC.

10. (Amended) The system of claim 5 wherein the signal conditioning stage generates a signal responsive to the sequence of analog signals.

11. (Amended) The system of claim 5 wherein the DAC receives one digital input signal per operating cycle and the analog signals are output at a non periodic rate over the operating cycle.

12. (Amended) The system of claim 11 wherein the analog signals have a periodic effect on an output of the signal conditioning stage.

13. (Amended) A method comprising:

receiving a multi-bit digital signal;

generating at least two analog signals including a first analog signal that is indicative of a sum of values of bits in the multi-bit digital signal, and a second analog signal that is indicative of said sum of values of said bits in the multi-bit digital signal; and

filtering at least two of the at least two analog output signals, including the first analog signal and the second analog signal.

14. (Amended) The method of claim 13 wherein the at least two analog signals are substantially equal to one another.

A5 Cancel

15. (Amended) The method of claim 13 wherein the filtering comprises providing the at least two of the at least two analog signals to a switched capacitor filter.

A6

17. (Amended) A system comprising:

means for receiving a multi-bit digital signal;

means for generating at least two analog signals including a first analog signal that is indicative of a sum of values of bits in the multi-bit digital signal, and a second analog signal that is indicative of said sum of values of said bits in the multi-bit digital signal; and

means for filtering at least two of the at least two analog signals, including the first analog signal and the second analog signal.

18. (Amended) The system of claim 17 wherein the at least two analog signals are substantially equal to one another.

A7

20. (Amended) The system of claim 17 wherein the means for generating comprises a switched capacitor DAC.

Please add the following claims: ✓

A8

21. (New) The system of claim 1 wherein the first analog signal and the second analog signal are each indicative of a sum of values of all of the bits in the multi-bit digital signal.

22. (New) The system of claim 1 wherein the first analog signal and the second analog signal are substantially equal to each other.

23. (New) The system of claim 1 wherein the first analog signal and the second analog signal are not substantially equal to each other.

24. (New) The system of claim 1 wherein the at least two analog signals are each indicative of said sum of values of said bits in the multi-bit digital signal.

25. (New) The system of claim 1 wherein each of the at least two analog signals is indicative of a sum of values of all of the bits in the multi-bit digital signal.

26. (New) The system of claim 1 wherein the at least two analog signals are not all substantially equal to each other.

27. (New) The system of claim 1 wherein the signal conditioning stage generates a signal that is responsive to both the first analog signal and the second analog signal.

28. (New) The system of claim 1 wherein the signal conditioning stage generates a signal that is responsive to each of the at least two of the at least two analog signals.

29. (New) A method comprising:

receiving a multi-bit digital signal;

generating at least two analog signals including a first analog signal that is indicative of a sum of values of bits in the multi-bit digital signal, and a second analog signal that is indicative of said sum of values of said bits in the multi-bit digital signal; and

providing at least two of the at least two analog signals to a signal conditioning stage, the at least two of the at least two analog signals including the first analog signal and the second analog signal.

30. (New) The method of claim 29 wherein the first analog signal and the second analog signal are each indicative of a sum of values of all of the bits in the multi-bit digital signal.

31. (New) The method of claim 29 wherein the first analog signal and the second analog signal are substantially equal to each other.

32. (New) The method of claim 29 wherein the first analog signal and the second analog signal are not substantially equal to each other.

33. (New) The method of claim 29 wherein the at least two analog signals are each indicative of said sum of values of said bits in the multi-bit digital signal.

34. (New) The method of claim 29 wherein the at least two analog signals are each indicative of a sum of values of all of the bits in the multi-bit digital signal.

35. (New) The method of claim 29 wherein the at least two analog signals are substantially equal to each other.

36. (New) The method of claim 29 wherein the at ieast two analog signals are not substantially equal to each other.

37. (New) A method as in any of claims 13 or 29, further comprising generating a signal that is responsive to both the first analog signal and the second analog signal.

38. (New) A method as in any of claims 13 or 29, further comprising generating a signal that is responsive to each of the at least two of the at least two analog signals.

39. (New) A system comprising:

means for generating at least two analog signals in response to a multi-bit digital signal, the at least two analog signals including a first analog signal that is indicative of a sum of values of bits in the multi-bit digital input signal and a second analog signal that is indicative of said sum of values of said bits in the multi-bit digital signal; and

a signal conditioning stage that receives at least two of the at least two analog signals, including the first analog signal and the second analog signal.

40. (New) The system of claim 39 wherein the first analog signal and the second analog signal are each indicative of a sum of values of all of the bits in the multi-bit digital signal.

41. (New) The system of claim 39 wherein the first analog signal and the second analog signal are substantially equal to each other.

42. (New) The system of claim 39 wherein the first analog signal and the second analog signal are not substantially equal to each other.

43. (New) The system of claim 39 wherein the at least two analog signals are each indicative of said sum of values of said bits in the multi-bit digital signal.

44. (New) The system of claim 39 wherein the at least two analog signals are each indicative of a sum of values of all of the bits in the multi-bit digital signal.

45. (New) The system of claim 39 wherein the at least two analog signals are substantially equal to each other.

46. (New) The system of claim 39 wherein the at least two analog signals are not substantially equal to each other.

47. (New) A system as in any of claims 17 or 39, wherein the signal conditioning stage generates a signal that is responsive to both the first analog signal and the second analog signal.

48. (New) A system as in any of claims 17 or 39, wherein the signal conditioning stage generates a signal that is responsive to each of the at least two of the at least two analog signals.

49. (New) The system of claim 1 wherein the DAC comprises a switched capacitor network including at least two capacitors that share charge with one another, the first analog signal and the second analog signal comprising charge supplied from the at least two capacitors.

50. (New) The system of claim 27 wherein the DAC comprises a switched capacitor network including at least two capacitors that share charge with one another, the first analog signal and the second analog signal comprising charge supplied from the at least two capacitors.

51. (New) The system of claim 49 wherein the first analog signal and the second analog signal comprise charge supplied from the at least two capacitors during a single digital to analog conversion cycle of the switched capacitor network.

52. (New) A system as in any of claims 5 or 12 wherein the DAC comprises a switched capacitor network and more than one of the analog signals is generated during a single digital-to-analog conversion cycle of the switched capacitor network.

REMARKS

This Amendment is in response to the Office Action mailed on July 13, 2001 objecting to the specification and rejecting all of the claims (claims 1-20). As an initial matter, Applicants respectfully point out that the Office Action provides no rationale for the rejection of the claims, just a bold citation to a reference. Applicants should not have to guess at an Examiner's reasoning. An Office Action is incomplete without a detailed application of the prior art to the claims being rejected. Nonetheless, in order to further prosecution, Applicants have made a good faith effort to respond to all of the rejections. To this effect, Applicants' Attorney initiated telephone interviews with Examiner Phan on October 8, 2001 and October 9, 2001. Applicants appreciate the courtesy shown by Examiner Phan in those telephone interviews. **However, if the Examiner believes, after this amendment, that the application is not in condition for allowance, Applicants request the courtesy of a new, non-final office action that completely addresses each and every feature of any rejected claims and explicates the factual basis for each rejection.**